IN THE CLAIMS

Please amend the claims to read as indicated herein.

1. (currently amended) An automated test equipment (ATE) comprising:

~~a tester per pin architecture having~~ a plurality of ~~individual decentralized~~ per-pin testing units, wherein each ~~per pin testing unit is for testing a respective pin of a device under test (DUT) by~~ of said plurality of per-pin testing units is configurable for at least one of emitting a signal to, or receiving a signal from, a pin of a device under test (DUT) having a plurality of DUT pins, ~~stimulus response signals to said respective DUT pin and receiving stimulus response signals from said respective DUT pin,~~ and wherein, during a testing sequence, ~~the~~ said DUT is defined as ~~one or more DUT cores representing one or more functional units of said DUT and including one or more DUT pins of said DUT~~ (a) a first DUT core that represents a first functional unit of said DUT and (b) a second DUT core that represents a second functional unit of said DUT~~; and~~;

means for assigning, during said testing sequence, ~~one or more~~ a subset of said plurality of per-pin testing units to ~~one or more ATE ports, wherein each ATE port comprises one or more of said per pin testing units and represents an independent functional testing unit for testing one or more of said DUT cores during said testing sequence,~~ an ATE-port, for interfacing with said first DUT core via a subset of said plurality of DUT pins; and

means for programming said ATE-port with a program for testing said first DUT core~~wherein at least one of said ATE ports includes programming means for independently defining,~~

wherein said program defines at least one of programming timing ~~and~~ or a stimulus/response pattern, and ~~wherein said programming means includes means for specifying~~ specifies a per-pin timing in terms of sets of available waveforms for each ~~ATE pin of the one~~ of said plurality of per-pin testing units assigned to said ATE-port, wherein each waveform represents a

sequence of events of various types occurring at specified instances in time, and wherein said program is independent of a program for testing said second DUT core.

2. (currently amended) The automated test equipment of claim 1, wherein said means for assigning comprises:

~~switching~~ means for switching connections between one or more of said plurality of per-pin testing units and one or more of said ~~DUT pins,~~ plurality of DUT pins; and

~~controlling~~ means for controlling ~~the~~ said switching ~~of said switching means~~ in accordance with ~~the~~ said assigning of said ~~one or more of the~~ subset of said plurality of per-pin testing units ~~to said one or more ATE ports during said testing sequence~~.

3. (canceled)

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4. (currently amended) The automated test equipment of claim 1, wherein said programming means comprises at least one of:

means for specifying cycle times of stimulus and response vectors for said ~~at least one~~ ATE-port;

means for specifying a pattern program for ~~the one~~ said ATE-port;

means for specifying a per-pin vector data for each ~~pin of the one ATE port~~ of said plurality of per-pin testing units assigned to said ATE-port; and

means for specifying analogue set-up conditions for analogue pins of ~~the one~~ said ATE-port.

5. (currently amended) The automated test equipment of claim 1, wherein said programming means comprises:

main pattern programs for implementing access protocols to said first DUT core ~~one or more of said DUT cores through a shared set of per pin testing units comprising one individual ATE port comprising at least per pin testing units~~

~~that are part of the ATE ports utilized to access said one or more DUT cores, and~~

~~independent pattern programs for implementing stimulus and response patterns for each DUT core of said one or more DUT cores~~.

6. (currently amended) The automated test equipment of claim 5, wherein said main pattern program comprises at least one of:

means for configuring said ~~one individual~~ ATE-port for activating said subset of said plurality of per-pin testing units ~~thereof~~ for accessing said ~~one or more DUT cores~~ first DUT core; and

means for selecting pattern data generated by pattern programs of said ~~accessed DUT cores~~ first DUT core during one testing sequence for testing said ~~accessed DUT cores~~ first DUT core.

7. (currently amended) The automated test equipment of claim 1, wherein said programming means comprises:

~~specifying~~ means for specifying an alias mapping between said plurality of per-pin testing units for a plurality of ~~said~~ ATE-ports, for specifying at least one of timing information and a pattern program of ~~one individual~~ said ATE-port to apply for ~~the~~ said plurality of ~~the~~ ATE-ports for which ~~the~~ said alias mapping is defined.

8. (currently amended) The automated test equipment according to claim 1, further comprising ~~specifying~~ means for specifying overall test conditions for a test that concurrently operates on multiple ATE-ports.

9. (currently amended) The automated test equipment of claim 8, wherein the specifying means comprises at least one of:

means for determining a set of concurrently active ATE-ports during a defined testing sequence;

means for selecting ~~the~~ ATE-port test conditions for one or more ATE-pins, for selecting an ATE-port timing setup for one or more ATE-pins;

means for specifying global test conditions to express dependencies between pins of ~~the~~ said DUT and ~~the~~ said ATE; and

means for determining a multi-port pattern burst as a sequence of per-ATE-port pattern programs for each ATE-port.

10. (currently amended) A method for testing a device under test (DUT) with automated test equipment (ATE) having ~~a tester-per-pin architecture having~~ a plurality of ~~individual decentralized~~ per-pin testing units, wherein each of said plurality of per-pin testing ~~unit is~~ units is configurable for at least one of emitting a signal to, or receiving a signal from, a pin of said DUT ~~for testing a respective pin of said DUT by at least one of emitting stimulus response signals to said respective DUT pin and receiving stimulus response signals from said respective DUT pin~~, said method comprising:

defining, for a testing sequence, ~~said DUT as one or more DUT cores representing one or more functional units of said DUT and including one or more pins of said DUT, and~~ (a) a first DUT core that represents a first functional unit of said DUT, and (b) a second DUT core that represents a second functional unit of said DUT;

assigning, during said testing sequence, ~~one or more of said~~ a subset of said plurality of per-pin testing units to ~~one or more ATE ports, wherein each ATE port comprises one or more of said per-pin testing units and represents an independent functional testing unit for testing one or more of said DUT cores during said testing sequence; and~~ an ATE-port, for interfacing with said first DUT core via a subset of said plurality of DUT pins; and

programming said ATE-port with a program for testing said first DUT core, wherein said program ~~defining~~ defines at least one of programming timing ~~and~~ or a stimulus/response pattern for ~~at least one of said ATE ports~~ said ATE-port, and specifying a per-pin timing in terms of sets of available waveforms for each ~~ATE pin of the~~ of said plurality of per-pin testing units assigned to said ATE-port, wherein each waveform represents a sequence of events of various

types occurring at specified instances in time, and wherein said program is independent of a program for testing said second DUT core.

11. (canceled)

12. (currently amended) The method of claim 10, wherein said defining at least one of programming timing and a stimulus/response pattern comprises at least one of:

specifying cycle times of stimulus and response vectors for ~~the one~~ said ATE-port;

specifying a pattern program for ~~the one~~ said ATE-port~~, preferably specifying common sequencing instructions for all per-pin testing units of the one ATE-port~~;

specifying per-pin vector data for each ~~per-pin testing unit of the one ATE-port~~ of said plurality of per-pin testing units assigned to said ATE-port; and

specifying analogue set-up conditions for analogue pins of ~~the one~~ said ATE-port.

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13. (previously presented) The method according to claim10, further comprising:

specifying overall test conditions for a test that concurrently operates on multiple ATE-ports.

14. (currently amended) The method of claim 13, wherein specifying overall test conditions comprises:

determining a set of concurrently active ATE-ports during a defined testing sequence;

selecting ~~the~~ ATE-port test conditions for one or more ATE-pins~~, preferably for selecting an ATE-port timing setup for one or more ATE-pins~~;

specifying global test conditions to express dependencies between pins of ~~the~~ said DUT and ~~the~~ said ATE~~, preferably global DUT specifications~~; and

determining a multi-port pattern burst as a sequence of per-ATE-port pattern programs for each ATE-port.

15. (currently amended) A data media for storing computer instructions for automated test equipment, said data media comprising:

instructions for testing a device under test (DUT) with automated test equipment (ATE) having ~~a tester per pin architecture having~~ a plurality of ~~individual decentralized~~ per-pin testing units, wherein each of said plurality of per-pin testing ~~unit is for testing a respective pin of said DUT by at least one of emitting stimulus response signals to said respective DUT pin and receiving stimulus response signals from said respective DUT pin~~ units is configurable for at least one of emitting a signal to, or receiving a signal from, a pin of said DUT, wherein said DUT includes a plurality of DUT pins;

instructions for defining, for a testing sequence, ~~said DUT as~~ a first DUT core that represents a first functional unit of said DUT, and (b) a second DUT core that represents a second functional unit of said DUT; ~~one or more DUT cores representing one or more functional units of said DUT and including one or more pins of said DUT~~; and

instructions for assigning, during said testing sequence, ~~one or more of said~~ a subset of said plurality of per-pin testing units to an ATE-port, ~~one or more ATE ports, wherein each ATE port comprises one or more of said per pin testing units and represents an independent functional testing unit for testing one or more of said DUT cores during said testing sequence; and~~ for interfacing with said first DUT core via a subset of said plurality of DUT pins; and

instructions for programming said ATE-port with a program for testing said first DUT core,

wherein said program ~~defining~~ defines at least one of programming timing ~~and~~ or a stimulus/response pattern for ~~at least one of said ATE ports~~ said ATE-port, and ~~specifying~~ specifies a per-pin timing in terms of sets of available waveforms for each ~~ATE pin of the~~ of said plurality of per-pin testing units assigned to said ATE-port, wherein each waveform represents a sequence of events of various types occurring at specified instances in time; and wherein said program is independent of a program for testing said second DUT core.

Please add the following claims, newly numbered as claims 16 - 19.

16. (new) An automated test equipment (ATE), comprising:

a plurality of per-pin testing units, wherein each of said plurality of per-pin testing units is configurable for at least one of emitting a stimulus signal to, or receiving a response signal from, a pin of a device under test (DUT) having a plurality of DUT pins, and wherein, during a testing sequence, said DUT is defined as having a first functional unit and a second functional unit;

means for assigning a subset of said plurality of per-pin testing units to an ATE-port for interfacing with said first functional unit via a subset of said plurality of DUT pins; and

means for programming said ATE-port with a program for testing said first functional unit,

wherein said program is independent of a program for testing said second functional unit.

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17. (new) An automated test equipment (ATE), comprising:

a plurality of per-pin testing units, wherein each of said plurality of per-pin testing units is configurable for at least one of emitting a stimulus signal to, or receiving a response signal from, a pin of a device under test, and wherein, during a testing sequence, said DUT is defined as having a first functional unit and a second functional unit; and

an ATE-port that receives a program for testing said first functional unit, and interfaces with said first functional unit via a subset of said plurality of per-pin testing units.

18. (new) The ATE of claim 17,

wherein said ATE-port is a first ATE-port, and said subset is a first subset, and

wherein said ATE further comprises a second ATE-port that receives a program for testing said second functional unit, and interfaces with said second functional unit via a second subset of said plurality of per-pin testing units.

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19. (new) The ATE of claim 18, wherein said program for testing said first functional unit is independent of said program for testing said second functional unit.